UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,053	01/31/2001	Giora Biran	CH9-2000-0037	6037

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EXAMINER
KENNEDY, LESA M

ART UNIT	PAPER NUMBER
2151	

DATE MAILED: 04/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2001*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☒ All　b)☐ Some * c)☐ None of:

　　　1.☒ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
　　　　application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
　　Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
　　Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1.   This action is responsive to the application filed on January 31, 2001. Claims 1-12 are

pending examination. Claims 1-12 are directed towards a system and method for a data

communications interface.

2.   Claim 9 has a grammatical error on line 25. Appropriate correction is recommended.

Drawings

3.   The drawings are objected to under 37 CFR 1.84(o) because:

   a.   Figs. 1-2 and 4-8 contain items that do not have descriptive legends.

   b.   The legend for item 20 in Fig. 1 is misspelled.

 A proposed drawing correction or corrected drawings are required in reply to the Office action

to avoid abandonment of the application. The objection to the drawings will not be held in

abeyance.

Specification

4.   The disclosure is objected to because the **Adapter Memory** section refers to Figure 3

(see line 1), but describe items shown in Figure 4.   Appropriate correction is required.

Claim Objections

5.   The numbering of claims is not in accordance with 37 CFR 1.126 which requires the

original numbering of the claims to be preserved throughout the prosecution. When claims are

canceled, the remaining claims must not be renumbered. When new claims are presented, they

must be numbered consecutively beginning with the number next following the highest

numbered claims previously presented (whether entered or not).

Misnumbered claims 11-13 been renumbered 10-12. A copy of the renumbered claims is

attached to this Office Action. Applicant is reminded to amend claims 11-12 to have the proper

dependencies.

Claim Rejections - 35 USC § 102

6.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on
sale in this country, more than one year prior to the date of application for patent in the United States.

7.   Claims 1-4 and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Short

(U.S. Patent No. 5,633,865).

As to claim 1, Short teaches a data communications interface for a node of a data

processing network, the interface comprising:

a transmission channel for communicating data from the node to the network (Fig. 1; col.

3, lines 3, 54; Short discloses a LAN channel (transmission channel) for transmitting data);

a transmission processor connected to the transmission channel for controlling flow of

data through the transmission channel (Fig. 1, element 18: MAC1; col. 3, lines 3 and 22; Short

discloses a MAC (transmission processor) for controlling the transmission of data packets to a

LAN);

a reception channel for communicating data from the network to the node (Fig. 1, col. 3,

lines 3, 54; Short discloses a LAN channel (reception channel) for receiving data);

a reception processor connected to the reception channel for controlling flow of data

through the reception channel (Fig. 1, element 18: MAC1; col. 3, lines 3 and 22; Short discloses

a MAC (reception processor) for controlling the reception of data packets from a LAN)

a shared memory (Fig. 1; element 24)

a local bus providing access to the shared memory by the transmission and reception

processors (Fig. 1, element 32: MAC bus; col. 3, lines 25-31).

As to claim 2, Short teaches the system of claim 1, wherein the shared memory comprises

a store for control information to be used by the transmission and reception processors in

controlling said flows of data (col. 3, lines 17-18; source address table as control information).

As to claim 3, Short teaches the system of claim 1, comprising a communication path for

communicating information between the transmission and reception processors via the shared

memory (Fig. 1; col. 3, lines 25-31).

As to claim 4, Short teaches the system of claim 1, comprising bus interface logic for

connecting the local bus, the transmission data channel, and the reception data channel to a bus

architecture of the node (Fig. 1, element 26 as bus architecture; Fig. 1, element 34 as bus

architecture of the node).

Claims 10-12 represent method claims that correspond to claims 1-3, respectively. They

do not teach or define any new limitations above claims 1-3, and therefore are rejected for

similar reasons.

Claim Rejections - 35 USC § 103

8.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

9.   Claims 5 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Short in

view of Kadambi et al. (U.S. Patent No. 6,707,818).

As to claim 5, Short teaches of:

the transmission processor being located in the transmission control path for controlling

communication of data (col. 3, lines 3, 22; Short discloses a MAC (transmission processor) for

controlling the transmission of data packets to a LAN channel), and

the reception processor being located in the reception control path for controlling

communication of data (col. 3, lines 3, 22; Short discloses a MAC (reception processor) for

controlling the reception of data packets from a LAN channel).

Short fails to teach the limitation of a transmission control path; transmission

segmentation logic for receiving a data frame, comprising a transmission header and a

transmission payload, from the node and supplying the transmission payload to the transmission

channel and the transmission header to the transmission control path; the transmission processor

controlling communication of data from the transmission payload to the network via the

transmission channel in dependence on the transmission header; a reception control path;

reception segmentation logic for receiving a data packet, comprising a reception header and a

reception payload, from the network and supplying the reception payload to the reception

channel and the reception header to the reception control path; and, the reception processor

controlling communication of data from the reception payload to the node via the reception

channel in dependence on the reception header.

However, Kadambi teaches these limitations. Kadambi teaches:

a transmission control path (col. 8, lines 7-10; Kadambi discloses a P-channel

(transmission control path));

transmission segmentation logic for receiving a data frame (col. 7, lines 56-67; Kadambi

discloses an MMU (transmission segmentation logic) that manages packets (data frames)),

comprising a transmission header and a transmission payload (col. 8, lines 1-10; Kadambi

discloses that a packet (data frame) comprises data (transmission payload) and a header), from

the node and supplying the transmission payload to the transmission channel and the

transmission header to the transmission control path (col. 8, lines 1-10; Kadambi discloses that

the data (payload) is sent on the C-channel (transmission channel), and the header is sent on the

P-channel (transmission control path));

the transmission processor controlling communication of data from the transmission

payload to the network via the transmission channel in dependence on the transmission header

(col. 8, line 7; Kadambi discloses that P-channel data (transmission payload) is sent

synchronously with the C-channel data (transmission header);

a reception control path (col. 15, lines 41-54; Kadambi discloses a P-channel (reception

control path);

reception segmentation logic for receiving a data packet (col. 14, lines 5-18; Kadambi

discloses that an ingress submodule (reception segmentation logic) receives incoming packets),

comprising a reception header and a reception payload (col. 14, lines 40-47; 61; Fig. 11;

Kadambi discloses that the first 64 bytes of the packet is the header information (reception

header), and the rest is data (reception payload)), from the network and supplying the reception

payload to the reception channel and the reception header to the reception control path (col. 15,

lines 41-54; Kadambi discloses placing data (reception payload) o the C-channel (reception

channel) and the corresponding message (reception header) on the P-channel (reception control

path); and,

the reception processor controlling communication of data from the reception payload to

the node via the reception channel in dependence on the reception header (col. 15, lines 41-54;

Kadambi discloses concurrently dispatching P-channel data (reception payload) and C-channel

data (reception header)).

It would have been obvious to one of ordinary skill in the art at the time of the invention

to modify Short in view of Kadambi so as to transmit and receive header and payload

information on separate channels. One would be motivated to do so to enable monitoring

transmitted packets.

As to claim 8, Short teaches the data communications interface of the invention

substantially as claimed (see rejection of claim 1 above).

Short fails to teach the limitation of a central processing unit; a memory; and, a bus

architecture interconnecting the central processing unit, the memory, and the data

communications interface.

However, Kadambi teaches the limitation of:

a central processing unit (Fig. 1; col. 4, line 66 – col. 5, line 28; CPU);

a memory (Fig. 1; col. 4, line 66 – col. 5, line 28; external memory); and,

a bus architecture interconnecting the central processing unit, the memory, and the data

communications interface (Fig. 1; col. 7, lines 14-16; bus).

It would have been obvious to one of ordinary skill in the art at the time of the invention

to modify Short in view of Muller so as to interconnect the data communications interface with a

CPU and external memory. One would be motivated to do so to (i) program the interface with

control packet processing rules via the CPU, and (ii) have additional memory when needed.

As to claim 9, Short teaches the system of claim 8, comprising a plurality of computer

systems and a network architecture interconnecting the computer systems (col. 1, line 10; Short

discloses a plurality of interconnected LANs).

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Short in

view of Muller et al. (U.S. Patent No. 6,061,362).

As to claim 6, Short teaches the invention substantially as claimed (see rejection of claim 1 above).

Short fails to teach the limitation of a network interface card comprising a printed circuit board and the data communications interface mounted on the printed circuit board.

However, Muller teaches the limitation of a network interface card comprising a printed circuit board and the data communications interface mounted on the printed circuit board (col. 4, lines 58-66; Muller discloses a network interface comprising a MII – media independent interface- (data communications interface) on an ASIC (printed circuit board)).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Short in view of Muller so as to have a network interface incorporating the data communications interface on an ASIC. One would be motivated to do so to enable interconnection between physical layer components and media access controllers.

As to claim 7, Short teaches the invention substantially as claimed (see rejection of claim 1 above).

Short fails to teach the limitation of an application specific integrated circuit comprising the interface.

However, Muller teaches the limitation of an application specific integrated circuit comprising the interface (col. 4, lines 58-66; Muller discloses a MII – media independent interface- (data communications interface) on an ASIC (printed circuit board)).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Short in view of Muller so as to incorporate the data communications interface onto an

ASIC. One would be motivated to do so to enable interconnection between physical layer

components and media access controllers.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Lesa Kennedy whose telephone number is (703) 305-8865. The

examiner can normally be reached on Monday - Friday, 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Glenton Burgess can be reached on (703) 305-4792. The fax phone number for the

organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 305-3900.

Lesa Kennedy
Art Unit 2151

CLAIMS

1.   A data communications interface for a node of a data processing network, the

5   interface comprising:

a transmission channel for communicating data from the node to the network;

a transmission processor connected to the transmission channel for controlling flow of

data through the transmission channel;

a reception channel for communicating data from the network to the node;

10   a reception processor connected to the reception channel for controlling flow of data

through the reception channel;

a shared memory; and,

a local bus providing access to the shared memory by the transmission and reception

processors.

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2.   An interface as claimed in claim 1 wherein the shared memory comprises a store for

control information to be used by the transmission and reception processors in controlling

said flows of data.

20 3.   An interface as claimed in claim 1 or claim 2, comprising a communication path for

communicating information between the transmission and reception processors via the shared

memory.

4.   An interface as claimed in any preceding claim comprising bus interface logic for

25 connecting the local bus, the transmission data channel, and the reception data channel to a

bus architecture of the node.

5.   An interface as claimed in any preceding claim, comprising:

a transmission control path;

30   transmission segmentation logic for receiving a data frame, comprising a transmission

header and a transmission payload, from the node and supplying the transmission payload to

the transmission channel and the transmission header to the transmission control path;

the transmission processor being located in the transmission control path for

controlling communication of data from the transmission payload to the network via the

transmission channel in dependence on the transmission header;

a reception control path;

5   reception segmentation logic for receiving a data packet, comprising a reception

header and a reception payload, from the network and supplying the reception payload to the

reception channel and the reception header to the reception control path; and,

the reception processor being located in the reception control path for controlling

communication of data from the reception payload to the node via the reception channel in

10 dependence on the reception header.

6.   A network interface card for insertion into a computer system, the network interface

card comprising a printed circuit board and a data communications interface as claimed in any

preceding claim mounted on the printed circuit board.

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7.   An application specific integrated circuit comprising an interface as claimed in any of

claims 1 to 5.

8.   A computer system comprising: a cental processing unit; a memory; a data

20 communications interface as claimed in any of claims 1 to 5; and, a bus architecture

interconnecting the central processing unit, the memory, and the data communications

interface.

9.   A data processing network comprising a plurality of computer systems as claimed in

25 claim 8 and a network architecture interconnected the computer systems.

10 11.   A method for communicating data to and from a node of a data processing network,

the method comprising:

communicating data from the node to the network via a transmission channel;

30 controlling flow of data through the transmission channel via a transmission processor

connected to the transmission channel;

communicating data from the network to the node via a reception channel;

controlling flow of data through the reception channel via a reception processor

connected to the reception channel; and,

    providing access to a shared memory by the transmission and reception processors via

a local bus.

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11 12.   A method as claimed in claim 11, comprising storing, in the shared memory, control

information to be used by the transmission and reception processors in controlling said flows

of data.

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10 13.   A method as claimed in claim 10 or claim 11, comprising communicating, via the

shared memory, information between the transmission and reception processors.